G Anusha, et al , International Journal of Computers Electrical and Advanced Communication Engineering (IJCEACE)™
Volume 1 , Issue 6, pp: 8 - 12, SEPTEMBER 2014.

A Novel Approach of 8-Bit Fast Radix-2 DCT Algorithm Using CORDIC

G.Anusha 1*, N.Satyanarayana 2*

1. *II.M.Tech (VLSI), Dept of ECE, AM Reddy Memorial College of Engineering & Technology, Petlurivaripalem.*
2. *Asst.Prof, Dept. of ECE, AM Reddy Memorial College of Engineering & Technology, Petlurivaripalem.*

ABSTRACT

In this paper presents an effective approach for design and implementation of eight-point DCT approximation based on coordinate rotation digital computer algorithm (CORDIC). Aim of this design is to make critical path of corresponding circuits can shorter, and reduce the delay of proposed technique. The proposed algorithm signal flows of DCTs and inverse DTs are developed for orthogonal property. This letter provides an easy way to implement this algorithm in digital image processing application.

Key words: DCT, CORDIC, Critical Path.

I. INTRODUCTION

The last two decades the field of Digital image and signal processing has been demonstrated by microprocessors. The designers provides with the advantage of single cycle multiply accumulate instructions as well as special addressing modes. The processors are very simple, flexible, and cheap they are relatively slow when it comes to performing certain criteria demanding digital signal processing tasks e.g. Digital Image processing , image compression, video processing, and digital communication for rapid advancements have been made in the field of VLSI and IC design. A result of special propose processors
with custom-architectures have come up. Higher speeds can be achieved by these customized hardware solutions at competitive costs. To add to this, various simple and hardware-efficient algorithms exist which map well onto these chips and can be used to enhance speed and flexibility while performing the desired signal processing tasks. One such simple and hardware-efficient algorithm is CORDIC, an acronym for Coordinate Rotation Digital Computer, proposed by Jack E Volder. CORDIC uses only Shift-and-Add arithmetic with table Look-Up to implement different functions. Since it uses only shift-add arithmetic, VLSI implementation of such an algorithm is easily achievable.

Implementing DCT using CORDIC algorithm to reduce the number of computations during processing to increases the accuracy of reconstruction of the images and to reduces the chip area of implementation of a processor built for this purpose. This reduces the overall power consumption. FPGA provides the hardware environment in which dedicated

processors can be tested for their functionality. They perform various high-speed operations that cannot be realized by a simple microprocessor. Primary advantage that FPGA offers is on- site programmability. It forms the ideal platform to implement and test the functionality of a dedicated processor designed using CORDIC algorithm.

II. PROPOSED DCT AND IDCT ALGORITHM BASED CORDIC

In existing system, for an 8-point signal DCT is defined. In post scaling neglecting the factor without loss of generality of main N-point DCT operation is described. The lifting based approach was showed that fast and accurate approximations of DCT can be obtained without using any multiplication. The family of such transforms differing in accuracy and efficiency has been called the binDCT.

Multiplier less implementation of plane rotation is CORDIC algorithm also considered. The performance maximization was of interest especially from hardware implementation point of view. This paper presents a novel family of CORDIC based algorithm with short critical path.

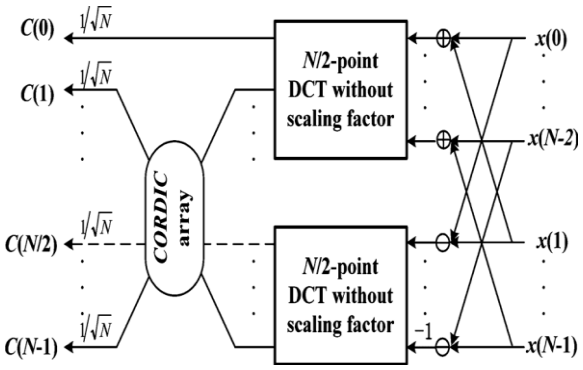

Fig. 1. Signal flow of an N-point fast discrete cosine transformation (DCT)

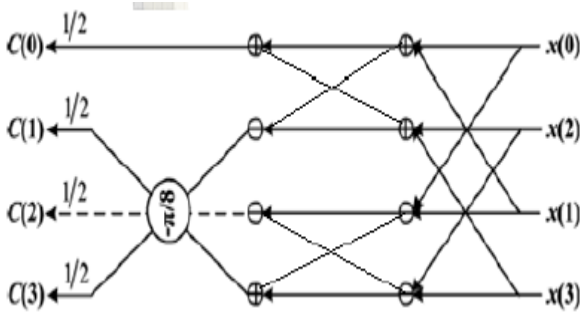

Fig.2. signal flow of 4-point fast discrete cosine transformation (DCT)

CORDIC Algorithm Figures:

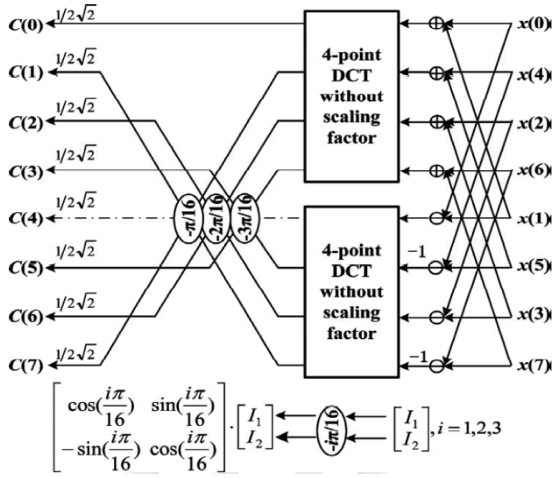

Fig.3. signal flow of 8-point fast discrete cosine transformation (DCT)

The proposed fast DCT algorithm signal flow graph is shown in fig.1. while the signal flow graphs of 4-point, and 8-point DCT are respectively as shown in fig.2. , and fig.3. The angles in the circles are used to represent the CORDICs with various rotation angles. The point connectivity inputs are given in bit reverse order and then outputs are in normal order.

For that reconstruction the IDCT is needed for signal flow graph of 8-point ICDT is shown in fig.4. Here the inputs are given in normal order and the outputs are in bit reverse order. This proposed CORDIC algorithm is highly suitable for VLSI implementation is built using shift registers and adders only. The proposed lifting scheme based fast multiplier less approximation of the DCT using only binary shift and addition operations.

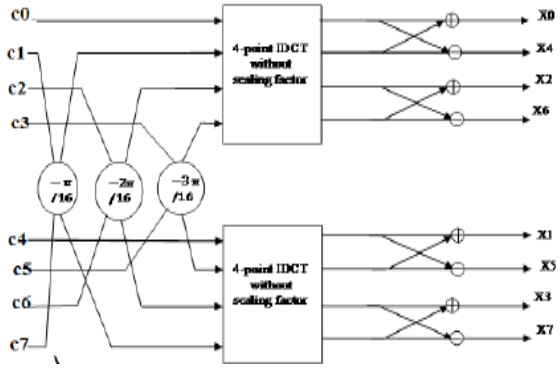

Fig.4. signal flow of 8-point inverse discrete cosine transformation (IDCT).

III. SIMULATION RESULTS

The proposed method of approximation DCT realized with the FPGA place and route (PAR) process to determine the exact hardware cost. We use Xilinx Virtex series of FPGA for our experimentation. The hardware cost is measured as the total number of slices required to implement the design

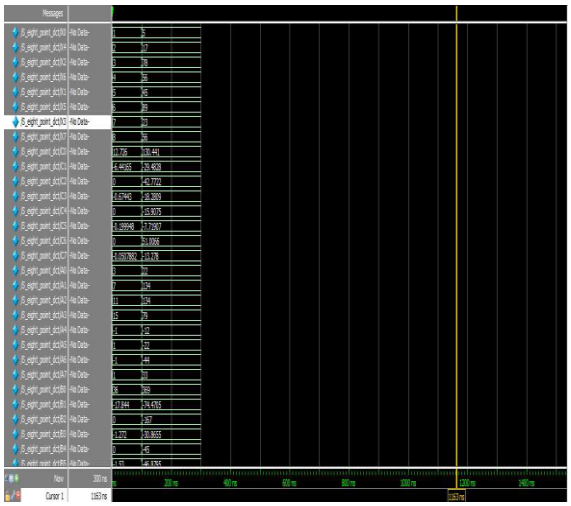

Fig.5. simulated output of 8-Point DCT.

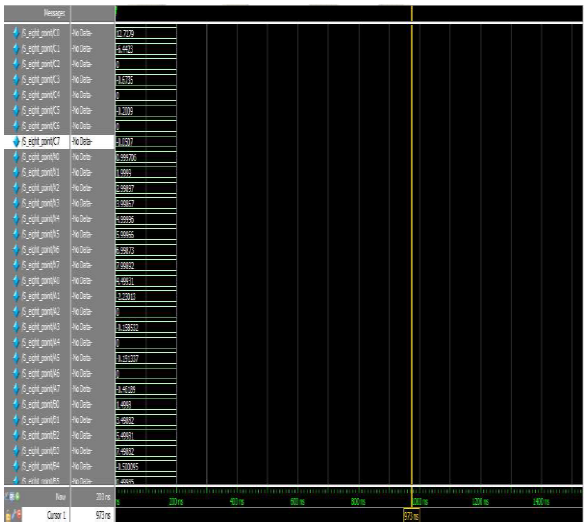

Fig. 6. Simulated output of 8-point DCT.

IV. CONCLUSION

A novel CORDIC based radic-2 fast DCT and IDCT algorithm is proposed in this paper. In can generate the next higehr order DCT from two identical lower order DCTs. Then compared to existing algorithms our proposed DCT and IDCT algorithms have sevarla advantages has low complexity , highly scalable, regular, and modular then able to dmit efficient pipelined implementation. Also it can be implemented in Digital image processing application thought the selected image pixel values is obtained through MATLAB software. Based on pixel values of the image we can apply to input for DCT and its output is given to the IDCT then it gives compressed pixel valuesas the ouput . further we can extend the 16-point DCT and IDCT comparision in future.

REFERENCES

[1]. E. Feig and S.Winograd, (Sep.1992) " algorithms for the discrete cosine transform, "IEEE Trans. Signal Process., vol. 40, no. 9, pp. 2174–2193.
[2]. L. Xiao and H. Huang, (Aug. 2012) " CORDIC based unified architecture for DCT and IDCT," in 2012 Int. Conf. Optoelectronics and Microelectronics (pp. 496–500).
[3]. N. Ahmed, T. Natarajan, and K. R. Rao,(1974) "Discrete cosine transform," IEEE Trans. Comput.,vol. C-23, pp. 90–94.
[4]. J. Liang and T. D. Tran, (2001) "Fast multiplierless approximations of the DCT with the lifting scheme," IEEE Trans. Signal Process., vol. 49, no. 12, pp. 3032–3044.
[5]. C. W. Kok, (Mar. 1997) "Fast algorithm for computing discrete cosine transform,"IEEE Trans. Signal Process., vol. 45, no. 3, pp. 757–760.
[6] T.D. Tran, The binDCT: fast multiplierless approximation of the DCT, IEEE Processing Lett., vol. 7 no. 6, pp. 141-144, 2000.
[7] M. Parfieniuk, Shortening the critical path in CORDIC-based approximation of the eight-point DCT, International Conference on Signal and Electronic Systems (ICSEC-2008), Krakow, Poland, September 14-17, pp. 405-408.
[8] B. Heyne, C.C. Sun, J. Goetze, S.J. Ruan, A computationally efficient high-quality CORDIC based DCT, 14th European Signal Processing Conference (Eusipco2006), Florence, Italy, 4-8 September 2006, pp. 11-15.
[9] S. Yu, E.E. Swartzlander Jr., A scaled DCT architecture with the CORDIC algorithm, IEEE Transactions on Signal Processing, vol.50, no. 1, pp. 160-167.
[10] C.-C. Sun, S.-J. Ruan, B. Heyne, and J. Goetze, Low-power and high-quality

CORDIC-based Loeffler DCT for signal processing, IET Circuits Devices Syst., vol. 1, no. 6, pp.623-655, 2007.